

Charge Trap Memory Based on Few-Layered Black Phosphorus

Qi Feng[†], Faguang Yan[†], Wengang Luo, and Kaiyou Wang^{*}

SKLSM, Institute of Semiconductors,
Chinese Academy of Science, Beijing 100083, China

^{*}To whom correspondence should be addressed; E-mail: kywang@semi.ac.cn

[†] These authors contributed equally to the work

Atomically thin layered two-dimensional materials, including transition-metal dichalcogenide (TMDC) and black phosphorus (BP), (*I*) have been receiving much attention, because of their promising physical properties and potential applications in flexible and transparent electronic devices . Here, for the first time we show non-volatile charge-trap memory devices, based on field-effect transistors with large hysteresis, consisting of a few-layer black phosphorus channel and a three dimensional (3D) Al_2O_3 / HfO_2 / Al_2O_3 charge-trap gate stack. An unprecedented memory window exceeding 12 V is observed, due to the extraordinary trapping ability of HfO_2 . The device shows a high endurance and a stable retention of $\sim 25\%$ charge loss after 10 years, even drastically lower than reported MoS_2 flash memory. The high program/erase current ratio, large memory window, stable retention and high on/off current ratio, provide a promising route towards the flexible and transparent memory devices utilising atomically thin two-dimensional materials. The combination of 2D materials with traditional high- k charge-trap gate stacks opens up an exciting field of nonvolatile memory devices.

Introduction

Nonvolatile memory cells, which are essential components for digital, portable and self-standing electronics, attract more and more attention, since the miniaturization, low power consumption and reliable data storage are highly desirable to solve the problem of large data capacity, integration density. Memories based on ultrathin layered two-dimensional (2D) materials like graphene and transition-metal dichalcogenides (TMDCs), such as MoS_2 , even graphene-oxide which can act as field effect transis-

tor (FET) channel, charge-trapping layer or electrode, have been demonstrated and considered to be promising candidates, due to their fantastic electronic properties and potential applications (1–8). It was shown that the large hysteresis in the gate characterization curves of FETs can be applied for memory devices operation. Despite the extremely high mobility in graphene, the absence of a band gap hinders the achievement of a high ON/OFF ratio (1, 9). This has led to intensive research in other 2D materials that have an intrinsic band gap. Among them, TMDCs, such as MoS₂ and WS₂, which have finite band gaps, not only have enabled the fabrication of high-performance field-effect transistor (FET) devices but have also paved the way for the realization of novel optoelectronic and valleytronic devices (10–15). Recently, black phosphorus monolayer, as well as its multilayers have been extensively studied (16–24). Comparing with TMDCs which have relatively low mobility, black phosphorus (BP) becomes an outstanding new element 2D layered material, with high mobility value of 1000 cm²V⁻¹s⁻¹ and 3900 cm²V⁻¹s⁻¹ at room temperature and low temperature, respectively (25, 26). BP is a van der waals type semiconducting layered material with a direct band gap of 0.3eV (bulk) to 2eV (monolayer), depending on the number of layers (27). The superior ambipolar property, higher mobility than TMDCs, comparable drain current modulation up to 10⁵ with TMDCs, promise black phosphorus as a good candidate for memory devices (25, 28–31). Moreover, nonvolatile memory based on black phosphorus also hold great promise for future flexible and transparent devices because of the mechanical flexible and tunable electronic properties of black phosphorus (32–34).

The selection of charge trapping layer and dielectrics is also significant because the applications of nonvolatile memory are still constrained by low charge retention and high operating voltage. In recent years, different structures of the memory devices have been investigated, by using graphene, MoS₂ or high-*k* oxide dielectric such as HfO₂, HfAlO, HfON and TiO₂ as the trapping layer (2, 3, 5, 35–38). The related works indicate the high efficiency and potential application of HfO₂ used as charge trapping layer (39–42). Meanwhile, a high quality dense tunneling dielectric and high-*k* blocking layer can provide low charge leakage and reduce the operating voltage as well as power consumption, respectively. Therefore, thanks to the high- HfO₂ as the trapping layer while the Al₂O₃ of different thickness as the tunneling and blocking layer, the structure of Al₂O₃/HfO₂/Al₂O₃ (AHA) gate stack can be utilised effectively in nonvolatile memory to obtain devices with excellent properties, such as

good trap ability, low power consumption and outstanding thermal stability (3, 41, 42). However, to our knowledge, there is no black phosphorus involved nonvolatile memory device being reported yet. We expect to enhance the performance of memory devices by combining the few-layer black phosphorus with conventional $\text{Al}_2\text{O}_3/\text{HfO}_2/\text{Al}_2\text{O}_3$ gate stack.

In this paper, we demonstrate memory devices fabricated from black phosphorus and high- k HfO_2 . As expected, the device shows a significant hysteresis and a substantial memory window thanks to the superior trap capacity of the $\text{Al}_2\text{O}_3/\text{HfO}_2/\text{Al}_2\text{O}_3$ (AHA) gate stack. Meanwhile, a robust charge retention of 70% retain after 10 years and stable endurance of more than 1200s and 120 cycles are obtained. The application of the conventional $\text{Al}_2\text{O}_3/\text{HfO}_2/\text{Al}_2\text{O}_3$ gate stack renders a possibility for a massive production of high-performance of black phosphorus-based 2D memory devices.

Results and discussion

Few-layer black phosphorus is obtained through mechanical exfoliation from black phosphorus bulk crystals onto prepatterned $\text{SiO}_2/\text{Si}^{++}$ substrates with the thickness of SiO_2 of 300 nm (25). We chose the particular flake with a thickness of 15 nm, as confirmed by atomic force microscopy, as extremely thin flakes (<5 nm) have a low mobility of $\sim 10 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ (17, 44). Source and drain contacts of 5 nm/85 nm Ti/Au were deposited *via* thermal evaporation. Subsequently, the $\text{Al}_2\text{O}_3/\text{HfO}_2/\text{Al}_2\text{O}_3$ (AHA) gate stack was grown *via* an atomic layer deposition (ALD) system with layer thickness of 5/8/35 nm, respectively. More details of device fabrication process can be found in the Methods.

A typical device schematic is shown in Fig.1(a). The non-Ohmic contact was indicated in Fig.1(b) and sublinear dependence of I_{sd} was clear in the small range as shown in the inset. An applied top-gate voltage (V_{TG}) modulates the amount of charge stored in the HfO_2 charge-trap layer, causing the variation of the conductivity of the BP channel. A back-gate voltage (V_{BG}) was applied to the degenerately doped silicon substrate to tune the memory characteristics by systematically shifting the Fermi level of black phosphorus. We noted that through the ALD deposition process the device performance can be significantly improved because of the thermal annealing under vacuum (19, 45). Also, the encapsulation of black phosphorus in a high- k dielectric environment will reduce the Coulomb scattering and modify the phonon dispersion in few-layer black phosphorus. Moreover, the oxide capping would protect the BP

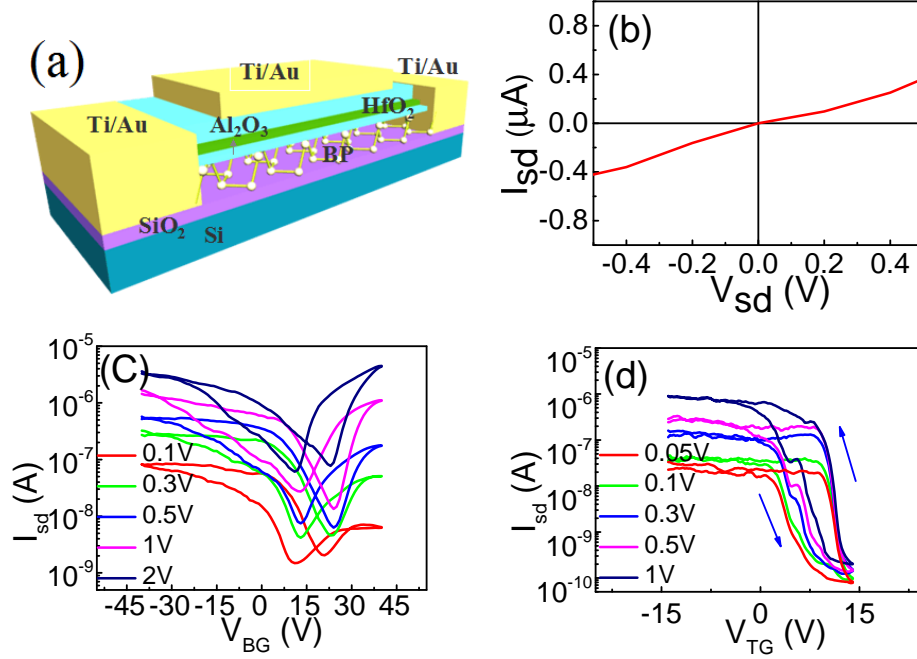


Figure 1: (Color Online) **Black Phosphorus Device Characterisation** (a) Device structure. The few-layer BP and 8-nm HfO_2 serve as the channel and the trap layer, respectively. (b) The output characteristics (I_{sd} - V_{sd}) of the device in logarithm scale. Inset shows the IV curve in linear scale within smaller voltage scale. (c) Transfer curves of the device with the back gate, sweeping between -40 V and 40 V, and (d) transfer curves of the device with the top gate, sweeping between -15 V and 15 V, with different source-drain voltage as denoted. The sweeping direction is denoted as blue arrows.

from ambient degradation (46,47). The black phosphorus in our device is measured to be about 15 layers by atomic force microscopy. The transfer curve (I_{DS} - V_{TG}) of the device can be obtained by sweeping V_{TG} while keeping the back gate grounded. When V_{BG} is swept between -40 to +40 V, the appearance of the hysteresis between the forward and backward sweep curves indicates the interface effect from SiO_2 and the black phosphorus channel, as shown in Fig.1(c).

The transfer characteristics were explored to probe the storage capability of the black phosphorus memory device. As shown in Figure 1(d), with $V_{BG} = 0$ V and different V_{sd} between 50mV and 1V, the transfer characteristic curves were obtained by sweeping V_{TG} from -15V to +15V, then back to -15V, and a maximal on/off ratio about 10^4 was acquired. A large memory window of about 12 V was observed, primarily originated from a large amount of electrons and holes stored in the charge-trap layer of HfO_2 . The mobility degradation is likely due to the thickness of 15 nm of BP. When different voltage sweep rates are applied, negligible appreciable differences are noted in transfer curves. It indicates that

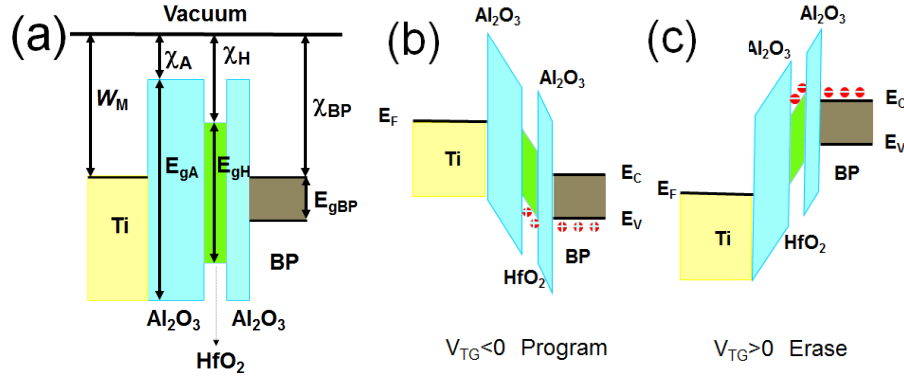


Figure 2: (Color Online) **Band diagram of BP memory device** (a) Band diagram of the BP-CTM memory cell with the AHA stack. (b) Band diagram of the program/erase state of the device under negative and positive V_{TG} . Negative V_{TG} programs the device. Holes tunneling from the few-layer black phosphorus channel are accumulated in the HfO₂ charge-trap layer. Positive V_{TG} erases the device. Electrons tunnel from the few-layer BP channel to the HfO₂ charge-trap layer.

the hysteresis of the transfer curve is not caused by the captured molecules, such as a thin layer of water, at the interface of BP/Al₂O₃ (48). The observed large gate hysteresis can be utilized for a nonvolatile memory device operation employing the BP layer as the channel.

The band diagram of the BP CTM with the AHA stack is shown in Figure 2. The electron affinity of Al₂O₃ and HfO₂ are 1eV and 2.5 eV, and the band gap are 7.7 eV and 4.9 eV, respectively (as shown in Fig.2(a)). The electron affinity of BP is about 4.4 eV and the band gap of bulk and monolayer BP are 0.3 eV and about 1.0 eV, respectively. In this situation, electron and hole potential well will be formed in the AHA stack layers structure, which can trap electrons and holes. In consideration of the 5 nm thick Al₂O₃, electrons can tunnel through the Al₂O₃ barrier by means of the mechanism of Fowler-Nordeim tunneling (49). In the device, the 5nm Al₂O₃-layer acts as tunnel layer, while 8nm HfO₂-layer acts as trap layer.

As presented in Fig.2(b,c), negative and positive gate voltage applied to the top gate correspond to the program and erase states in the device operation process, respectively. In the program process, the shape of the energy band changes as shown in Fig.2 and the barrier of the tunneling oxide layer which is close to the BP film becomes thin enough for tunneling; hence, holes in BP layer can be pulled and transferred to HfO₂-layer through the Al₂O₃ tunnel layer as a result of the Fowler-Nordeim tunneling effect (see Fig.2). The resultant accumulation of holes in HfO₂ will shift the threshold voltage (V_{th}) to the negative direction, since this accumulation of holes in the HfO₂ layer would screen the top-gate

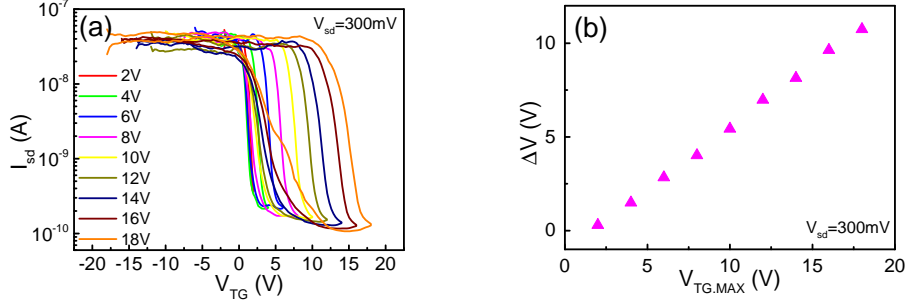


Figure 3: (Color Online) **Charge-Trap Memory Window** (a) I_{sd} - V_{TG} characteristics under different $V_{TB,MAX}$ at $V_{sd}=300$ mV. (b) Extraction of memory window *vs* $V_{TB,MAX}$. The memory window increases from ~ 1 to ~ 12 V in our experimental settings.

electric field effect. When the gate voltage is swept toward a higher positive value, the holes in trap layer will be pushed back to the BP channel; meanwhile, the electrons in conduction band of BP will be pulled into the trap layer which also can screen the top-gate electric field and cause the threshold voltage shifted to the positive direction (see Fig.2). Then, an appreciable memory window can be obtained in the transfer characteristic curve as a result of the capability of electron and hole trapping from AHA stack. As the top-gate voltage changes from positive to negative, the memory cell works in the program state, while as the top-gate voltage changes from negative to positive, the memory cell works in the erase state.

The amount of charge stored in the charge-trap layer can be modulated by gradually changing the maximum ($+V_{TG,MAX}$) and minimum ($-V_{TG,MIN}$) voltage applied on the top gate. Figure 3(a) shows the enlarged hysteresis window when $|V_{TG,MAX}|$ becomes larger. The shift of the threshold voltage toward negative and positive direction corresponds to the hole and the electron trapping, respectively. The increased threshold voltage shift (ΔV) as a function of $V_{TG,MAX}$ is summarized in Figure 3(b). The amount of charge stored in the charge-trap layer can be estimated from the expression:

$$n = \frac{\Delta V C_{HF-AL}}{e} \quad (1)$$

where e is the electron charge, ΔV is the threshold voltage shift toward the negative or the positive direction compare to the original transfer curve (50). According to Figure 3(a), the hysteresis window of the sweep between -2 and +2 V is close to zero, thus it can be defined as the original transfer curve, corresponding to no tunneled electrons or holes existing in the charge-trap layer. $C_{HF-AL} = \epsilon_0 \epsilon_{AL} / d_{AL}$ is the capacitance between the HfO_2 charge-trap layer and the top gate, where ϵ_0 is the vacuum permittivity,

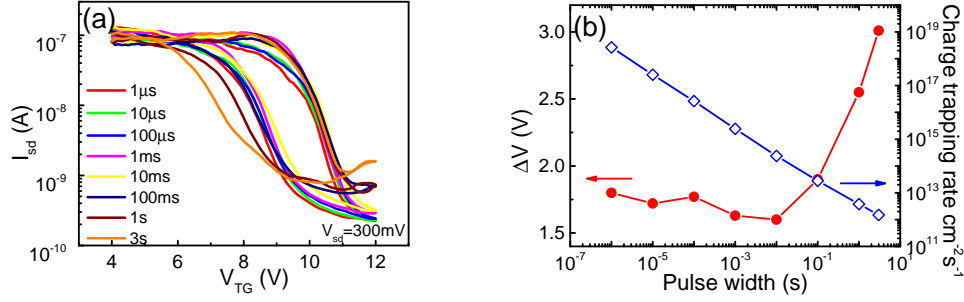


Figure 4: (Color Online) **Dynamic Transition rate of the BP memory device** (a) Transfer curves of I_{sd} - V_{TG} in a narrow range of +4 ~ +12 V under different pulse duration (-16V, 1 μ s to 3 s). (b) Extracted threshold voltage shift and calculated charge trap rate as a function of the pulse width, ranging between 1 μ s and 3s.

ϵ_{AL} and d_{AL} are the relative dielectric constant (~ 8) and thickness (~ 35 nm) of the Al_2O_3 blocking layer, respectively.

Here, we define $\Delta V = \Delta V_h + \Delta V_e$, where ΔV_h and ΔV_e are the threshold voltage shift toward the negative and positive direction compare to the original transfer curve, corresponding to the density of stored holes and electrons, respectively. The calculated density of stored electrons and holes under $-V_{TG.MAX}$ of 18V is on the order of 10^{14} and 10^{13} cm^{-2} , respectively, which is in agreement with previously reported memory devices using graphene or graphene oxide as charge-trap layers (5, 7, 8). The lower tunneling barrier height of electrons than holes is accounted for the high trap density of electrons.

To study the dynamic transition rate of the black phosphorus memory device, a positive pulse (+16 V, duration of 3s) was applied to the top gate ($V_{BG} = 0$) to set the device in the erase state, followed by a -16 V pulse with different duration time. The reading procedure was performed by sweeping I_{DS} - V_{TG} in a very small range (+4 to +12 V) to minimize the effect of the measurements to the device's state. After each reading operation, a positive pulse (+16 V, duration of 3s) was applied on the top gate to reset the device in the erase state. The threshold voltage shift ΔV_{TH} was acquired by applying in a linear fit to the linear regime of the reading I_{DS} - V_{TG} curve. Figure 4(a) shows a clear shift of the threshold voltage when the width of the pulse is changed to 10 ms, which sets a reference for the following dynamic behaviour measurements. ΔV_{TH} shows nearly a saturation behaviour when the pulse width increases to 3 s (Figure 4(a)). The charge-trapping rate can be estimated from the expression:

$$\frac{dN_{trap}}{dt} = \frac{C_{HF-AL}}{e} \times \frac{\Delta V_{TH}}{\Delta t} \quad (2)$$

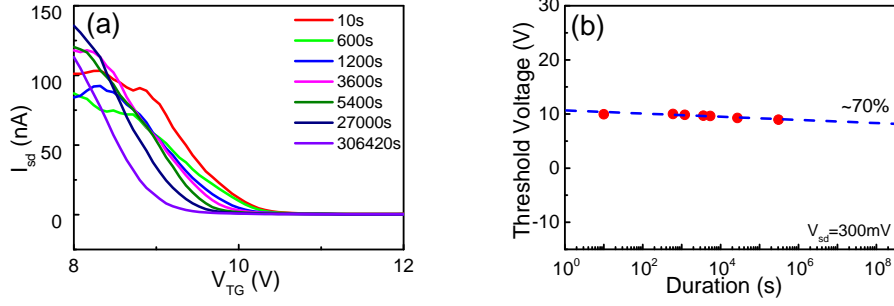


Figure 5: **Retention characteristics of the BP memory device** (Color Online) (a) The transfer curves (I_{sd} - V_{TG}) swept in different time intervals.(b) Retention time of the threshold voltage. The programming pulse is set to be -16V with 1s duration. Threshold voltage was obtained by linearly fitting to the transfer curves. We estimate that only 30% of the charges will be lost after 10 years.

Table 1: Comparison of future memory device performance

	Our work	2D Memory MoS ₂	2D memory Graphene	2D memory Graphene	Organic memory	Organic memory
Channel material	Black phosphorus	MoS ₂	Graphene	Graphene	pentacene	P3HT
Charge trapping layer	HfO ₂	Graphene (few-layer)	MoS ₂ (few-layer)	GO	Au nano-crystal monolayer	Cu NPs
Barrier	Al ₂ O ₃	Al ₂ O ₃ /HfO ₂	h-BN	Poly-vinylphenol	Al ₂ O ₃	PS or PVN
Memory window	12V from ± 18 V	8V from ± 15 V	17V from ± 40 V	11.7V from ± 20 V	2.25V from ± 5 V	42.6V from ± 50 V
Endurance	~ 120	~ 120	~ 100	~ 200	1000	~ 100
Retention (/10 years)	30%loss	70%loss	70%loss	—	40%loss per day	80%loss
Operating power	$V_{sd}=300$ mV Pulse; ± 16 V	$V_{sd}=50$ mV Pulse; ± 18 V	$V_{sd}=100$ mV Pulse; ± 40 V	$V_{sd}=1.5$ V Pulse; ± 20 V	$V_{sd}=3$ V Pulse; ± 5 V	$V_{sd}=20$ V Pulse; ± 50 V
Sample size						
Lateral size	~ 5 μ m	~ 5 μ m	~ 5 μ m		~ 1 mm	inches
Thickness	~ 15 nm	~ 1 nm	~ 10 nm	~ 1 nm	~ 30 nm	

where ΔV_{TH} is the threshold voltage shift and Δt is the pulse width (2). The calculated charge-trapping rate varies from 10^{19} to 10^{12} $\text{cm}^{-2}\text{s}^{-1}$ when the pulse width changes from 1 μ s to 3 s. The reason for such a high charge-trap rate is because of the thin Al₂O₃ tunnel layer (only 5 nm), which makes electron/hole charges much easier to tunnel through.

The retention characteristics of the device are determined by the height of the tunneling barrier and the depth of potential well formed in the Al₂O₃/HfO₂/Al₂O₃ charge-trap stack (40, 51). Figure 5(a) shows the threshold voltage at different time intervals after programming the device with a negative pulse (-16 V, duration of 1s). The transfer curve was also obtained in a small voltage range (+4 to +12 V). The extracted threshold voltage ΔV_{RTH} varies from 4.5 to 3.4 V after 10^6 s(Figure 5(b)), from which we estimate that only 30 % of the charges will be lost after 10 years. The enhancement of the retention characteristics of our black phosphorus memory device is also related to the extraordinary trapping ability of the Al₂O₃/HfO₂/Al₂O₃ gate stack.

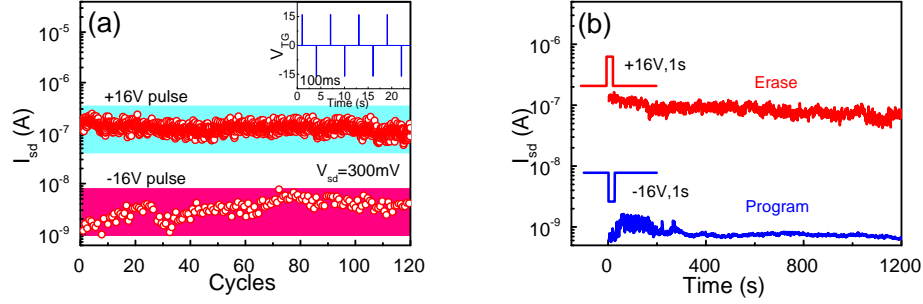


Figure 6: (Color Online) **Endurance of the BP memory device** (a) Endurance of the memory device for 500s, 120 cycles with the program/erase voltage being +16, 100ms and -16 V, 100ms. (b) The stability of program/erase state of the device after programming at +16V, 1s duration and erasing at -16V, 1s ($V_{sd}=300\text{mV}$). The negative part of the threshold voltage shift corresponds to the hole trapping which can be suppressed by the positive back-gate voltages, vice versa for the electron trapping in the positive part.

The retention of trapped charge data was then studied. Two states with different currents can be defined as ‘trap’ and ‘release’ states, corresponding to program state and erase state, respectively. The retention performance curve could show that if the trapped charge can be maintained without loss of charge. In addition, as shown in Fig.6(b), high $I_{\text{release}}/I_{\text{trap}}$ ratio of 10^2 can be obtained, comparing with memory device with floating gate utilising 2D materials, e.g. GBM. Most of devices measured in this work exhibit similar retention characteristics regardless of thickness of charge-trap layer and tunnelling barrier.

To test the endurance of the memory device, a sequence of pulse ($\pm 16\text{ V}$, duration of 100 ms) was applied to the top gate with $V_{BG} = 0$ while I_{DS} was measured ($V_{DS} = 300\text{ mV}$). As presented in Figure 6(a), the charge trapping can be preserved over 100 cycles. Most memory devices relying on charge trapping suffer from problems related to charge retention, such as loss of charge by back-tunnelling, injection of carriers of the opposite type or redistribution of charge in defects (52). The robustness and stability of the device shows a great perspective of applications in nonvolatile memory technology.

As 2D materials like graphene, MoS_2 , even graphene oxide have received much attention in view of their application for nonvolatile memory, organic memories also have been studied as leading contending devices for future memory devices (43, 53–56). Here, we compared the performances of our devices based on black phosphorus to those of reported memory devices based on other 2D materials and organic materials (Table 1). Compared with graphene and MoS_2 charge trapping memories, the memory devices

fabricated in our study display better performance with stable retention of 70% retain after 10 years, while the memory window and endurance comparable to these devices. In addition, in terms of memory window, retention, miniaturization and low energy consumption, the device discussed in our work is obviously superior than those of organic memories. So it is reasonable to believe that nonvolatile memory devices based on black phosphorus hold great promise for future flexible and transparent memory devices.

Conclusion

In conclusion, we have demonstrated a memory device based on few-layer black phosphorus and $\text{Al}_2\text{O}_3/\text{HfO}_2/\text{Al}_2\text{O}_3$ charge-trap stack. All the devices studied showed similar hysteresis characteristics, regardless of the channel length and BP film thickness. From the measurement of retention and endurance characteristics, it was confirmed that high- k dielectric HfO_2 layer acts as an effective charge-trapping layer in this configuration. High on/off current ratio of 10^2 , large memory window about 12 V at $V_{TG}=16\text{V}$, long data retention that only 30% charge loss after 10 years, were attained. This study provides a promising route towards the flexible and transparent memory devices, utilising ultrathin two-dimensional materials.

Experimental section

Device fabrication

Thin layers of black phosphorus were mechanically exfoliated on a silicon wafer with 300 nm-thick SiO_2 . The flakes were identified by a combination of optical and scanning electron microscopy (JEOL). We used multilayer BP with a thickness of ~ 15 nm and widths of around ~ 5 μm . The $\text{SiO}_2/\text{Si}^{++}$ is used as a back gate to control the carrier concentration in the BP. Source and drain electrodes of Ti (3 nm)/Au (85 nm) were fabricated on BP samples by standard electron-beam lithography (EBL), followed by thermal evaporation and metal lift-off techniques. Electrodes with width 0.3-0.8 μm and a channel length of 0.5-2 μm were used. The wafers were covered with polymethyl methacrylate (PMMA) e-beam resist immediately after exfoliation to avoid possible degradation upon longer exposure to air. After lift-off, stacked layers of $\text{Al}_2\text{O}_3/\text{HfO}_2/\text{Al}_2\text{O}_3$ (5/8/35 nm) were deposited *via* ALD. During the ALD process, trimethylaluminum and triakis (ethyl-methylamido) hafnium were reacted at 120 °C with

water for Al_2O_3 and HfO_2 , respectively. The top-gate (Ti/Au 3 nm/50 nm) electrodes were subsequently fabricated using another EBL and metal deposition process.

Characterization of BP material and device

Atomic force microscopy (Bruker Multimode 8) was used to ensure the qualities and total film thickness of black phosphorus. Electrical properties of fabricated devices were measured with a semiconductor parameter analyzer (Agilent, B1500A) in vacuum and at room temperature.

Supplementary

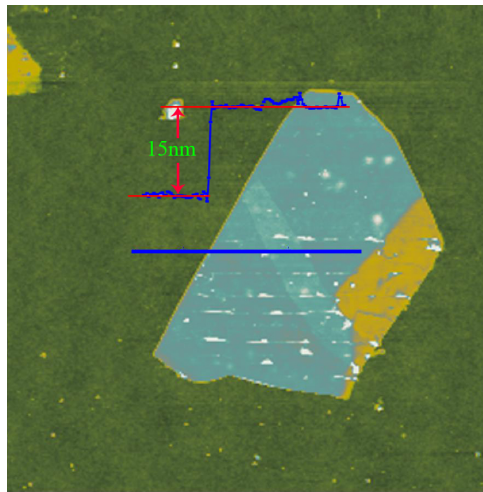


Figure 7: (Color Online) **AFM measurements**

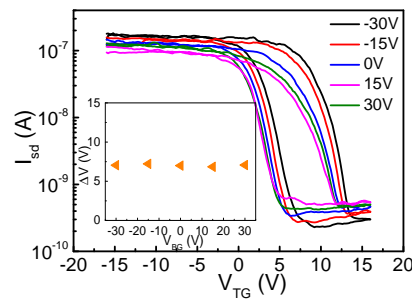


Figure 8: (Color Online) **Back-gate effect of the BP memory device**

Conflict of Interest

The authors declare no competing financial interest.

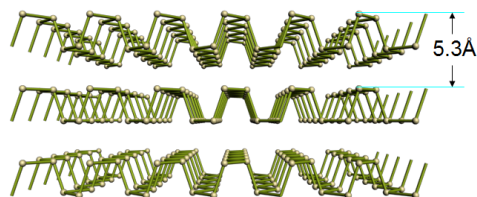


Figure 9: (Color Online) **Device schematic** (a) Schematic of the memory device based on BP-AHA, (b) structure schematic of the black phosphorus.

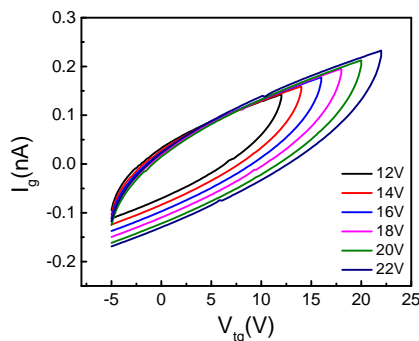


Figure 10: (Color Online) **Top-gate current leakage** Current leakage at different $V_{TG.MAX}$

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